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TITLE: CLOCK GENERATING CIRCUIT AND IMAGE FORMING DEVICE

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ABSTRACT:

PROBLEM TO BE SOLVED: To reduce influence on image quality owing to nonuniformity in a scanning light amount in an image forming device using a polygon mirror in a writing system and its clock generating circuit.

SOLUTION: The clock generating circuit is provided with a delay chain part 413 for minutely delaying a clock from an oscillator to be reference and generating multiple delay clocks, a synchronization detecting part 414 for selecting the multiple delay clocks (synchronization delay clock) in a synchronized state with an index signal from the delay chain part and outputting the delay stage number as synchronizing information, a table 402 for holding scanning light amount nonuniformity information concerning nonuniformity in the scanning light amount generated in an optical system means, a synchronization changeover part 415 for generating a select signal which decides from which phase the delay clock among the multiple delay clocks is selected through the use of the synchronization delay clock, the synchronizing information and the scanning light amount nonuniformity information and a signal selecting part 416 for selecting the delay clock corresponding to the select signal.

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